REPLY UNDER 37 CFR §1.116
EXPEDITED PROCEDURE
TECHNOLOGY CENTER 2800

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Chen-Bau Wu, et al	§	Attorney Docket No. 2003-0893 / 24061.148
Serial No.: 10/821,432	§	Customer No. 42717
Filed: April 9, 2004	§	Group Art Unit: 2815
For: A High Voltage Semiconductor Device Utilizing A Deep Trench Structure	§	Examiner: Budd, Paul A.
	§	Conf. No. 1237

AMENDMENT AFTER FINAL

Mail Stop AF
Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant is enclosing a Petition for a one-month time extension, along with the requisite extension fee. However, if any other fees are necessary, including additional extension of time fees, the extension of time is herby requested, and the Commissioner is herby authorized to charge any fees, including those for the extension of time, to Haynes and Boone, LLP's Deposit Account No. 08-1394.

In response to the Final Office Action dated February 13, 2006 and the Advisory Action dated May 22, 2006, please amend the above-identified application as follows:

Amendments to the Drawings begin on page 2 of this paper and replacement sheets are attached.

Amendments to the Claims are reflected in the listing of claims which begins on page 3 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Amendments to the Drawings

Applicant has corrected the title of each of the drawings and amended Figures 2 and 3. Replacement Sheets are attached.

Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1-9. (Canceled)

10. (Currently amended) ~~The semiconductor device of claim 4 further~~ A semiconductor device comprising:

a substrate including a source and drain, the source having a first edge and the drain having a first edge;

a gate between the source and drain, the gate having a first portion;

a first deep trench structure located directly under the first portion of the gate viewed in a direction from the gate to the substrate, and proximate to the first edge of the source and the first edge of the drain, wherein the first deep trench structure has a depth greater than 0.5 μm;

a neighboring semiconductor device; and

a first shallow trench isolation structure located between the semiconductor device and the neighboring semiconductor device.

11. (Original) The semiconductor device of claim 10 further comprising:

a second shallow trench isolation structure adjacent to the drain wherein the drain is situated between the first shallow trench isolation structure and the second shallow trench isolation structure.

12. (Original) The semiconductor device of claim 11 wherein the gate is extended to partially overlay the second shallow trench isolation structure.

13-26. (Canceled)

27. (Currently amended) ~~The semiconductor device of claim 21 further~~ A semiconductor device comprising:

a substrate including a source and drain, the source having a first edge and the drain having a first edge;

a gate electrode on the substrate and between the source and drain, a first portion of the gate electrode extending past the first edge of the source and the first edge of the drain;

a first deep trench structure located directly under the first portion of the gate electrode viewed in a direction from the gate electrode to the substrate and proximate to the first edge of the source and the first edge of the drain, wherein the first deep trench structure has a depth greater than 0.5 μm;

a neighboring semiconductor device; and

a first shallow trench isolation structure located between the semiconductor device and the neighboring semiconductor device.

28. (Original) The semiconductor device of claim 27 further comprising:

a second shallow trench isolation structure adjacent to the drain wherein the drain is situated between the first shallow trench isolation structure and the second shallow trench isolation structure.

29. (Original) The semiconductor device of claim 28 wherein the gate is extended to partially overlay the second shallow trench isolation structure.

30-41. (Canceled)

42. (Currently amended) ~~The semiconductor device of claim 37 further~~ A semiconductor device

comprising:

a substrate having a source and drain, having widths that are substantially equal and each having a first edge substantially located along a common line on the substrate;

a gate electrode on the substrate and between the source and the drain, the gate electrode having a first portion extending past the first edge of the source and the first edge of the drain;

a first deep trench structure located directly under the first portion of the gate electrode viewed in a direction from the gate electrode to the substrate, the first deep trench structure parallel to the common line on the substrate and proximate to the first edge of the source and the first edge of the drain, wherein the first deep trench structure is substantially deeper than 0.5 μm;

a neighboring semiconductor device; and

a first shallow trench isolation structure between the semiconductor device and the neighboring semiconductor device.

43. (Original) The semiconductor device of claim 42 further comprising:

a second shallow trench isolation structure adjacent to the drain wherein the drain is situated between the first shallow trench isolation structure and the second shallow trench isolation structure.

44. (Original) The semiconductor device of claim 43 wherein the gate is extended to partially overlay the second shallow trench isolation structure.

45-54. (Canceled)

Remarks:

The foregoing amendments cancel claims 1-9, 13-26, 30-41, and 45-54, but Applicant reserves the right to file a continuation application that presents the subject matter of these claims for further consideration on the merits. Reconsideration of presently pending claims 10-12, 27-29, and 42-44 is respectfully requested in light of the following amendments and remarks.

Applicant respectfully submits that the Advisory Action of May 22, 2006, incorrectly indicated that the period for the reply expires three months from the mailing date of the Final Rejection. The period for reply should have expired on the mailing date of the Advisory Action (May 22, 2006) since a response to the Final Rejection was filed within two months of the Final Rejection. (See MPEP §706.7(f)). The Final Rejection was mailed February 13, 2006 and the response to the Final was filed on April 13, 2006. Accordingly, Applicant is enclosing a Petition for a one-month time extension along with the requisite extension fee.

Objection to the Drawings

The title of each of the drawings has been corrected per the Examiner's suggestion. Figures 2 and 3 have been resubmitted with hatching per the Examiner's suggestion. Additionally, in Figure 3, reference numeral "**140**" has been amended to "**142**," reference numeral "**142**" has been amended to "**144**," and reference numeral "**144**" has been amended to "**146**." Figure 3 has been amended to be consistent with Figure 2 and the description in the Specification. No new matter has been added.

Allowable Subject Matter

Noted with appreciation is the indication in the Office Action of February 13, 2006, that claims 10-12, 27-29, and 42-44 are directed to allowable subject matter, and would be allowed if rewritten in independent form. Claims 10, 27, and 42 have been rewritten in independent form and are now in condition for allowance. Claims 11-12 depend from and further limit claim 10

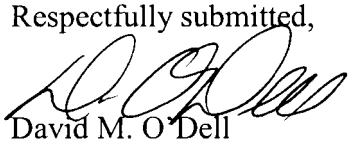
and are allowable as well. Claims 28-29 depend from and further limit claim 27 and are allowable as well. Claims 43-44 depend from and further limit claim 42 and are allowable as well.

Conclusion

The foregoing amendments are believed to place the present application in condition for allowance. An early formal notice of allowance of claims 10-12, 27-29, and 42-44 is respectfully requested.

Deposit account 08-1394 can be used for any over or under payments. Also, the Examiner is invited to call the undersigned at the phone number provided below as needed.

Respectfully submitted,

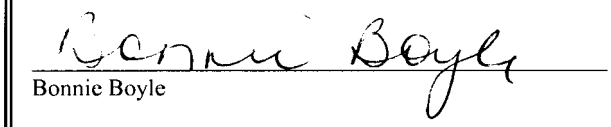


David M. O'Dell
Reg. No. 42,044

Date: June 19, 2006
HAYNES AND BOONE, LLP
901 Main Street, Suite 3100
Dallas, Texas 75202 3789
Telephone: 972.739.8635
Facsimile: 214.200.0853
Docket No.: 2003-0893 / 24061.148
Document No. R-138858.1

Certificate of Service

I hereby certify that this correspondence is being filed with the U.S. Patent and Trademark Office via EFS-Web on June 19, 2006.



Bonnie Boyle

Replacement Sheet

Attorney Docket No. 24061.148
UTILIZE DEEP TRENCH STRUCTURE TO PREVENT LDMOS FROM PARASITIC TURNING-ON CHANNELS

SHEET 1 OF 3

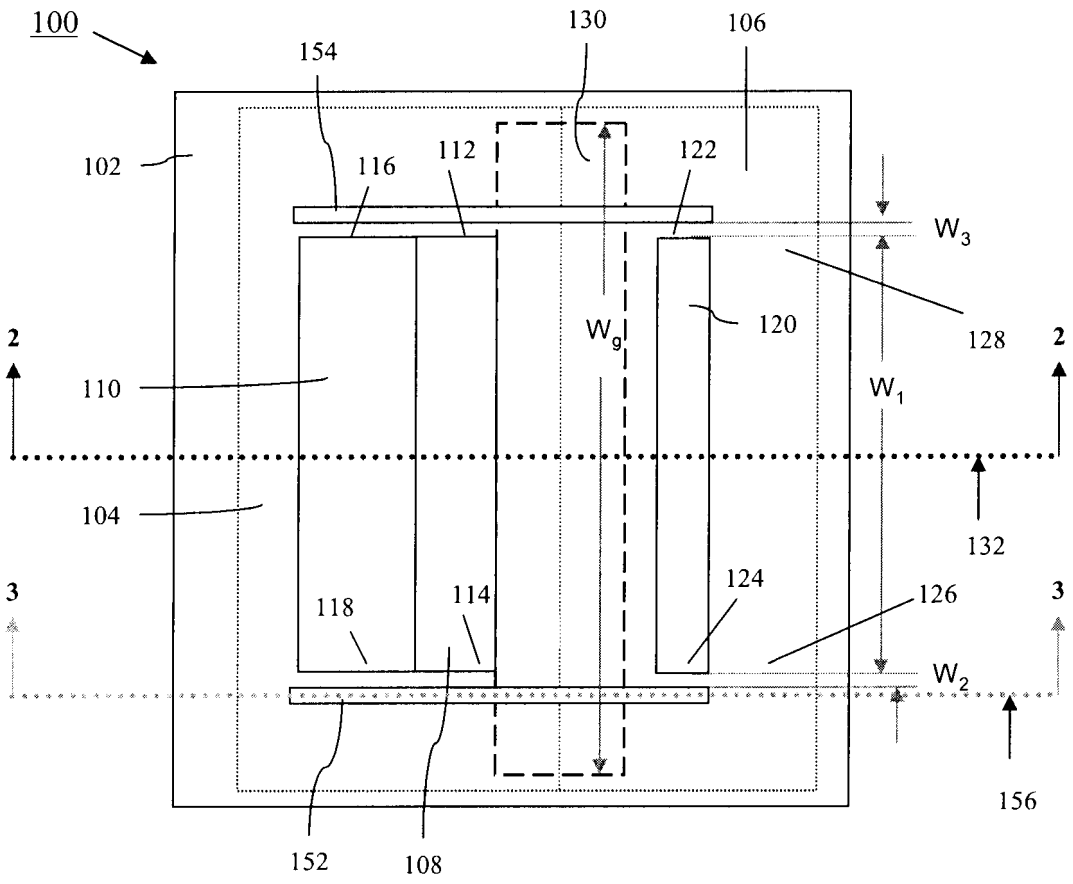


Fig. 1

Replacement Sheet

Attorney Docket No. 24061.148
UTILIZE DEEP TRENCH STRUCTURE TO PREVENT LDMOS FROM PARASITIC TURNING-ON CHANNELS

SHEET 2 OF 3

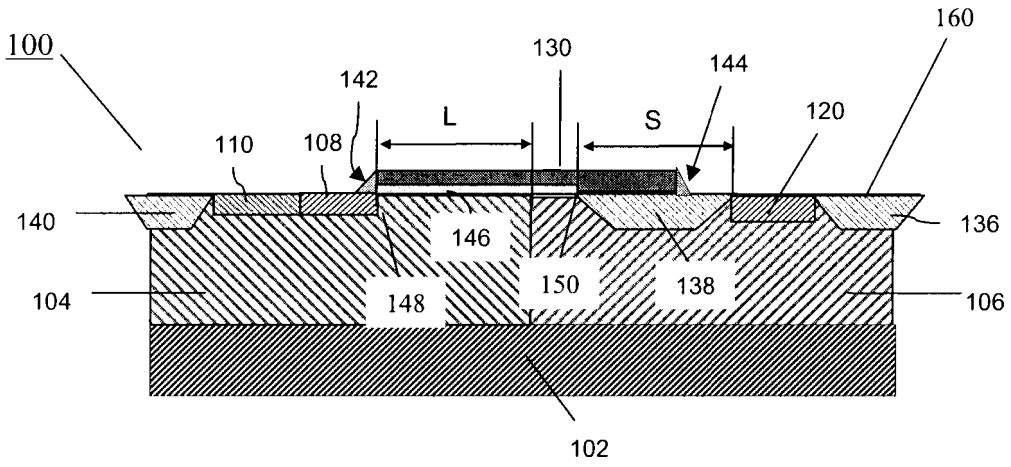


Fig. 2

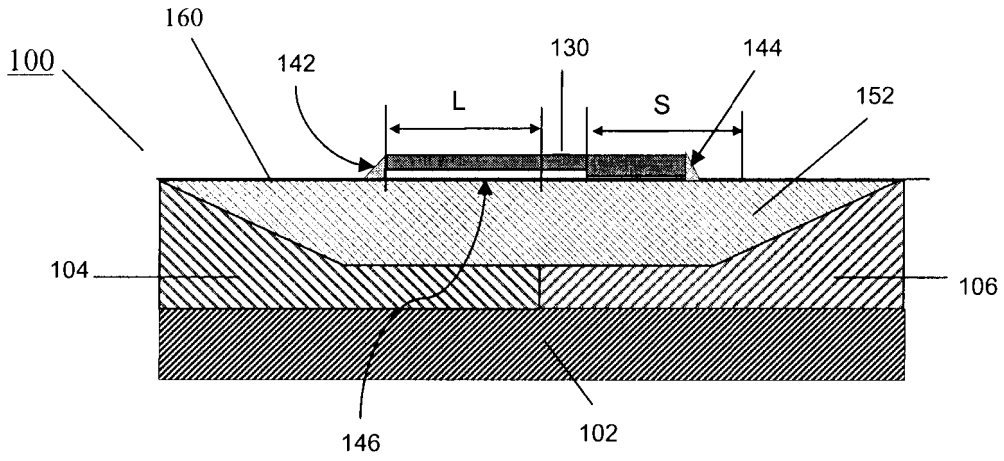


Fig. 3

Replacement Sheet

Attorney Docket No. 24061.148
UTILIZE DEEP TRENCH STRUCTURE TO PREVENT LDMOS FROM PARASITIC TURNING-ON CHANNELS

SHEET 3 OF 3

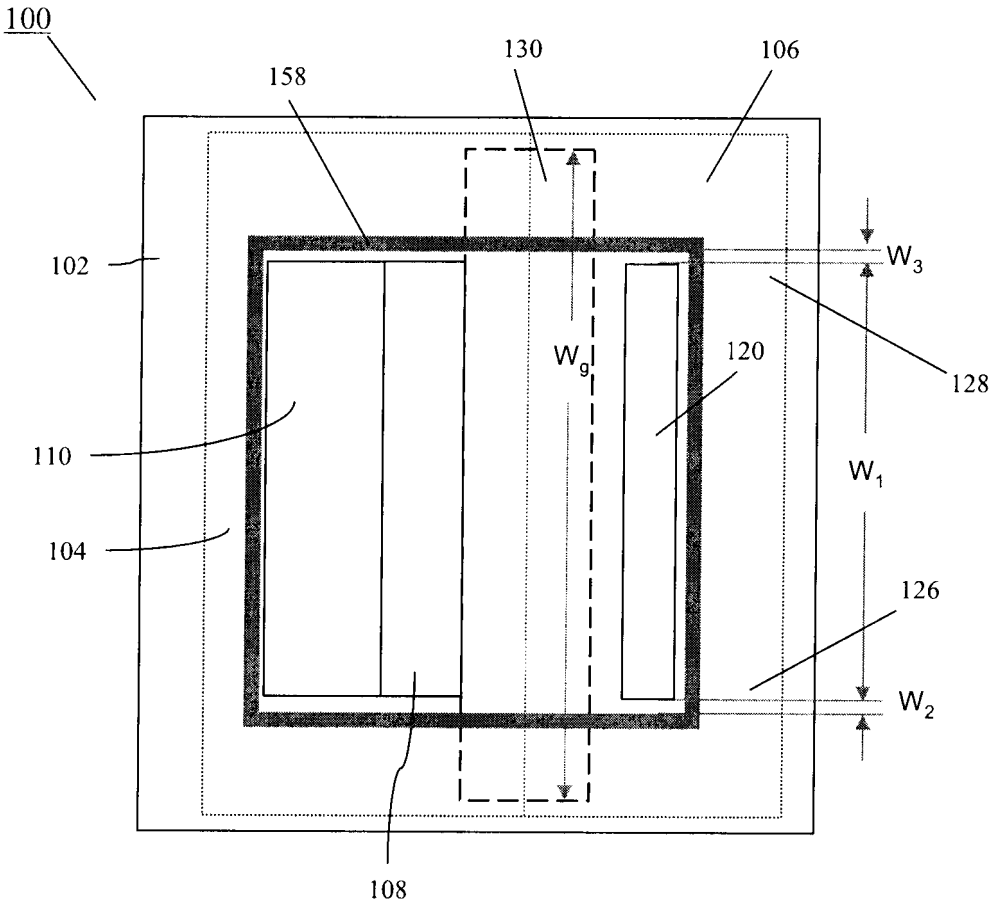


Fig. 4